Electronic Version
Stylesheet Version v1.1.1

Description

DYNAMIC DRIVER BOOST CIRCUITS

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] The present invention generally relates to driver circuits and more particularly to improved pull-up and pull down boost circuitry for drivers that minimizes block delay skew.

[0003] Description of the Related Art

[0004] As technology advances, device sizes get smaller. Likewise, maximum operating voltages decrease with each new technology. With smaller device sizes and a lower VDD, it becomes very difficult to improve block delay and reduce di/dt while still maintaining appropriate slew rates and keeping the design within the specifications. This invention tightens the slew rate and also minimizes block delay skew and jitter across different PVT conditions.

SUMMARY OF INVENTION

[0005] The invention begins with a driver circuit that includes a logical enable device and a driving transistor. In order to tighten slew rate and minimize delay skew, the invention adds a pull-down booster circuit connected to the gate of the driving transistor and/or a pull-up booster circuit connected to the gate of the driving transistor. The pull-down booster circuit is adapted to

kly start pulling down the voltage at the gate of the driving transistor when the voltage level at the input to the logical enable device changes from a first voltage (e.g., a logical "0") to a second higher voltage (e.g., a logical "1"). The pull-down booster than dynamically shuts itself off when the voltage level at feedback node G (the gate of the driving transistor) changes from a first voltage (e.g., a logical 1) to a second lower voltage (e.g. a logical 0). The voltage level at feedback node G (the gate of the driving transistor) only needs to fall to a threshold voltage below the voltage supply to start shutting off the pull-down booster. Thus, the stronger the pull-down booster circuit is, the faster it will shut itself off. This is why the pull-down boost circuit can be considered dynamic and sensitive to different process, temperature and voltage conditions. After the pull-down booster shuts off, the voltage level at the gate of the driving transistor is controlled by the logical enable device which controls the slew rate and di/dt by utilizing resistors in series with the CMOS FETS. By using only the resistors to control di/dt and slew rates, the circuit is adversely affected in terms of delay. By using the boost circuit in combination with the resistors, the invention is able to get a balance of delay, slew rate control, reduced di/dt, and less overshoot/undershoot voltage at the PAD. The pull-up booster circuit is adapted to dynamically pull-up the voltage at the gate of the driving transistor when the voltage level at the input to the logical enable device changes in the opposite direction.

[0006] The pull-down booster circuit has a logical NAND device having one input connected to an input signal supplied to the logical enable device. The pull-down booster circuit also includes a pull-down transistor that has its gate connected to the output of the NAND device, a source connected to the output of the logical enable device (and the gate of the driving transistor),

and a drain connected to ground. The second input of the logical NAND device is connected to the output of the logical enable device, such that the logical NAND device dynamically activates the pull-down transistor to pull-down the gate of the driving transistor to ground (e.g., a logical "0") only while the input signal supplied to the logical enable device is at the second voltage level (e.g., a logical "1") and the signal on the output of the logical enable device (and the gate of the driving transistor) is also at the second voltage level (e.g., a logical "1").

[0007] The pull-up booster circuit has a logical NOR device having one input connected to the input signal supplied to the logical enable device. The pull-up booster circuit also includes a pull-up transistor that has its gate connected to an output of the NOR device, a drain connected to an output of the logical enable device (and the gate of the driving transistor), and a source connected to the higher voltage level. The second input of the logical NOR device is connected to the output of the logical enable device (and the gate of the driving transistor), such that the logical NOR device activates the pull-up transistor to pull-up the gate of the driving transistor to the higher voltage level (e.g., a logical "1") only while the input signal is at the second voltage level (e.g., a logical "0") and the signal on the output of the logical enable device (and the gate of the driving transistor) is also at the second voltage level (e.g., a logical "0").

[0008] The invention can also provide at least one pull-down delay element between the logical NAND device and the pull-down transistor and at least one pull-up delay element between the logical NOR device and the pull-up transistor. The pull-down delay element is connected in parallel with the

signal line running between the logical NAND device and the pull-down transistor. The pull-up delay element is similarly connected in parallel with the signal line running between the logical NOR device and the pull-up transistor. This parallel arrangement provides that the delays created by the pull-down delay element and the pull-up delay element are dynamically varied depending upon the difference between the voltage level at the input to the logical enable device and the voltage level at the gate of the driving transistor.

[0009] If the pull-down transistor comprises a P-type transistor, it is directly connected to the logical NAND device. Similarly, if the pull-up transistor comprises an N-type transistor, it is also directly connected to the logical NOR device. Otherwise, if the pull-down transistor comprises an N-type transistor, the circuit further includes an inverter positioned between the logical NAND device and the pull-up transistor. Similarly, if the pull-up transistor comprises a P-type transistor, the circuit further includes an inverter positioned between the logical NOR device and the pull-up transistor.

BRIEF DESCRIPTION OF DRAWINGS

[0010] The invention will be better understood from the following detailed description of preferred embodiments with reference to the drawings, in which:

[0011] Figure 1 is a schematic diagram of a driver circuit that utilizes a pull-down booster according to the invention;

[0012] Figure 2 is a schematic diagram of a driver circuit that utilizes a pull-up booster according to the invention;

[0013] Figure 3 is a schematic diagram of a driver circuit that utilizes a pull-down booster and a pull-up booster according to the invention;

[0014] Figure 4 is a schematic diagram of a driver circuit that utilizes a pull-down booster according to the invention;

[0015] Figure 5 is a schematic diagram of a driver circuit that utilizes a pull-up booster according to the invention;

[0016] Figure 6 is a schematic diagram of a driver circuit that utilizes a pull-down booster and a pull-up booster according to the invention;

[0017] Figure 7 is a schematic diagram of a driver with dynamic feedback and a pull-up booster and pull-down booster according to the invention;

[0018] Figure 8 is a schematic diagram of a pull-down booster according to the invention;

[0019] Figure 9 is a schematic diagram of a pull-down booster according to the invention;

[0020] Figure 10 is a schematic diagram of a pull-down booster according to the invention;

[0021] Figure 11 is a schematic diagram of a pull-down booster according to the invention;

[0022] Figure 12 is a schematic diagram of a pull-up booster according to the

invention;

[0023] Figure 13 is a schematic diagram of a pull-up booster according to the invention;

[0024] Figure 14 is a schematic diagram of a pull-up booster according to the invention; and

[0025] Figure 15 is a schematic diagram of a pull-up booster according to the invention.

DETAILED DESCRIPTION

[0026] As mentioned above, there is a need to tighten the slew rate and also minimize block delay skew and jitter in driver devices. In order to reduce slew rate and minimize delay skew, the invention adds a pull-down booster circuit connected to the gate of the driving transistor and/or a pull-up booster circuit connected the gate of the driving transistor. As shown in Figure 1, the driver circuit includes a logical enable device 11 (such as a NAND logic circuit) and a driving transistor 12 such as a P-type transistor. The pull-down booster circuit 10 is adapted to dynamically pull-down the voltage at the gate of the driving transistor 12 when the voltage level at the input to the logical enable device 11 changes from a logical "0" to a logical "1". Feedback loop 14 provides dynamic feedback to the pull-down booster 10 from node G. The pull-down circuit 10 in Figure 1 will increase the speed with which the transistor 12 turns on, thus decreasing the output rise delay.

[0027] Similarly, as shown in Figure 2, the pull-up booster circuit 20 is adapted to dynamically pull-up the voltage at the gate of the driving transistor 12 when

the voltage level at the input to the logical enable device 11 changes from a logical "1" to a logical "0". Feedback loop 22 provides dynamic feedback to the pull-up booster 20 from node G. The pull-up circuit 20 in Figure 2 will increase the speed with which the transistor turns off, thus decreasing the output fall delay.

[0028] Figure 3 illustrates that the driver circuit can be equipped with both a pull-up booster 20 and a pull-down booster 10 to further reduce delay skew and slew rate. The circuit in Figure 3 has both a pull-up boost circuit and a pull-down boost circuit which will decrease both rise and fall delays. The pull-up boost and the pull-down boost will never be enabled at the same time.

[0029] While Figures 1-3 relate to a predriver logic circuit that utilizes a P-type field effect transistor (PFET), Figures 4-6 relate to a predrive logic circuit that utilizes an N-type field effect transistor (NFET). More specifically, Figures 4-6 illustrate that the inventive pull-down booster circuit 10 and pull-up booster circuit 20 can also be utilized with a logical enable device 40 (such as a NOR circuit) when the driving transistor 41 is an N-type transistor. As mentioned with respect to Figures 1-3, the predriver logic can include either the pull-down booster 10 (Figure 4), the pull-up booster 20 (Figure 5) or both the pull-up booster 20 and the pull-down booster 10 (Figure 6). Figure 7 demonstrates that the inventive pull-down booster circuit 10 and pull-up booster circuit 20 can also be utilized to dynamically boost the output of the PAD in a feedback structure that includes both the NFET and PFET devices.

[0030] More details regarding the pull-down booster circuit 10 are shown in Figures

8-11 and more details regarding the pull-up booster circuit 20 are shown in Figures 12-15, which are discussed in greater detail below.

[0031] As shown in Figure 8, one embodiment of the pull-down booster circuit 10 has a logical NAND device 80 having one input connected to an input signal A supplied to the logical enable device 11, 40. The pull-down booster circuit 10 also includes a pull-down transistor that has its gate connected to the output of the NAND device 80, a source connected to the output of the logical enable device G (and the gate of the driving transistor 12, 41), and a drain connected to ground.

[0032] The present invention improves block delay by immediately providing a boost as soon as driver input A switches from a first voltage to a second voltage (from high to low or from low to high, depending upon specific circuit design). The boost circuit dynamically shuts off as soon as predrive output G has risen/fallen. More specifically, the second input of the logical NAND device 80 is connected to the gate of the driving transistor 12, 41 (G), such that the logical NAND device 80 dynamically activates the pull-down transistor to pull-down the gate of the driving transistor 12, 41 to ground (e.g., a logical "0") only while the input signal A supplied to the logical enable device 11, 40 is at the second voltage level (e.g., a logical "1") and the signal on the output of the logical enable device 11, 40 G (and the gate of the driving transistor12, 41) is also at the same second voltage level (e.g., a logical "1") such that they are at the same logic level. Initially A=0, G=1 which means that the pull-down transistor is off. When input A switches from a logic "0" to a logic "1" (from low voltage to high voltage), there is a short period of time when A=1 and G=1. During this short period of time, the

pull-down transistor is on and the pull-down transistor helps pull G down to logic "0". When G becomes a "0", the pull-down transistor turns off and the boost circuit is finished boosting.

[0033] If the pull-down transistor comprises an N-type transistor 82 (as shown in Figures 8 and 10), the circuit further includes an inverter 81 positioned between the logical NAND device 80 and the pull-up transistor 82. To the contrary, if the pull-down transistor comprises a P-type transistor 90, as shown in Figures 9 and 11, the NAND device 83 is directly connected to the PFET 90. If the goal is for G to keep pulling down to zero quickly during the whole boost period, the invention uses the NFET 82 in Figure 8. If the goal is for G to slowly pull down to zero, the invention uses the PFET 90 in Figure 9. The PFET 90 passes a bad logic "0" below its threshold voltage (Vt) and stops passing a logic "0" when G reaches the threshold voltage of the PFET 90, which makes G pull down to zero more slowly than with the NFET 82 (which will remain conductive until the NAND device 80 shuts the NFET 82 off).

[0034] As shown in Figures 10 and 11, the invention can also provide at least one pull-down delay element (hystersis path) 100 between the logical NAND device 80 and the pull-down transistor 82, 90. By adding a hystersis path in the boost circuit, the invention has a prolonged period of time that the boost circuit is held on. The pull-down delay element(s) 100 is (are) connected in parallel with the signal line running between the logical NAND device 80 and the pull-down transistor 82, 90. This parallel arrangement provides that the delays created by the pull-down delay element(s) 100 are dynamically varied depending upon the difference between the voltage level at the input to the

logical enable device 11, 40 and the voltage level at the gate of the driving transistor 12, 41.

[0035] As shown in Figures 12-15, the pull-up booster circuit 20 has a logical NOR device 120 having one input connected to the input signal A supplied to the logical enable device 11, 40. The pull-up booster circuit 20 also includes a pull-up transistor that has its gate connected to an output of the NOR device 120, a drain connected to an output G of the logical enable device 11, 40 (and the gate of the driving transistor), and a source connected to the higher logic "1" voltage level.

[0036] The second input of the logical NOR device 120 is connected to the gate of the driving transistor 12, 41 (G), such that the logical NOR device 120 dynamically activates the pull-up transistor to pull-up the gate of the driving transistor 12, 41 to higher voltage (e.g., a logical "1") only while the input signal A supplied to the logical enable device 11, 40 is at the second voltage level (e.g., a logical "0") and the signal on the output of the logical enable device 11, 40 G (and the gate of the driving transistor12, 41) is also at the second voltage level (e.g., a logical "0") such that they are at the same logic level. Thus, initially, A=1, G=0 which means that the pull-up transistor is off. When input A switches from a logic "1" to a logic "0", there is a short period of time that A=0 and G=0. During this short period of time, the pull-up transistor is on and the pull-up transistor helps pull G up to logic "1". When G becomes a "1", the pull-up transistor turns off and the boost circuit is finished boosting.

[0037] As with the pull-down circuit 10, if the pull-up transistor comprises a P-type

transistor 122 (as shown in Figures 12 and 14), the circuit further includes an inverter 121 positioned between the logical NOR device 120 and the pull-up transistor 122. To the contrary, if the pull-up transistor comprises an N-type transistor 130, as shown in Figures 13 and 15, the NOR device 83 is directly connected to the PFET 90.

[0038] As shown in Figures 14 and 15, the invention can also provide at least one pull-up delay element 100 between the logical NOR device 120 and the pull-up transistor 122, 130. As discussed above, the pull-up delay element(s) 100 is (are) connected in parallel with the signal line running between the logical NOR device 120 and the pull-up transistor 122, 130, which provides that the delays created by the pull-up delay element(s) 100 are dynamically varied depending upon the difference between the voltage level at the input to the logical enable device 11, 40 and the voltage level at the gate of the driving transistor 12, 41.

[0039] Thus, as shown above, the invention begins with a driver circuit that includes a logical enable device and a driving transistor. In order to tighten slew rate and minimize delay skew, the invention adds a pull-down booster circuit connected to the gate of the driving transistor and/or a pull-up booster circuit connected to the gate of the driving transistor. The pull-down booster circuit is adapted to quickly start pulling down the voltage at the gate of the driving transistor when the voltage level at the input to the logical enable device changes from a first voltage (e.g., a logical "0") to a second higher voltage (e.g., a logical "1"). The pull-down booster than dynamically shuts itself off when the voltage level at feedback node G (the gate of the driving transistor) changes from a first voltage (e.g., a logical 1) to a second lower voltage (e.g.

a logical 0). The voltage level at feedback node G (the gate of the driving transistor) only needs to fall to a threshold voltage below the voltage supply to start shutting off the pull-down booster. Thus, the stronger the pull-down booster circuit is, the faster it will shut itself off. This is why the pull-down boost circuit can be considered dynamic and sensitive to different process, temperature and voltage conditions. After the pull-down booster shuts off, the voltage level at the gate of the driving transistor is controlled by the logical enable device which controls the slew rate and di/dt by utilizing resistors in series with the CMOS FETS. By using only the resistors to control di/dt and slew rates, the circuit is adversely affected in terms of delay. By using the boost circuit in combination with the resistors, the invention is able to get a balance of delay, slew rate control, reduced di/dt, and less overshoot/undershoot voltage at the PAD. The pull-up booster circuit is adapted to dynamically pull-up the voltage at the gate of the driving transistor when the voltage level at the input to the logical enable device changes in the opposite direction.

[0040] While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.